TECHINSIGHTS

QUICK LOOK ANALYSIS OF THE (COMPANY) PART#

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TECHINSIGHTS

October 2007

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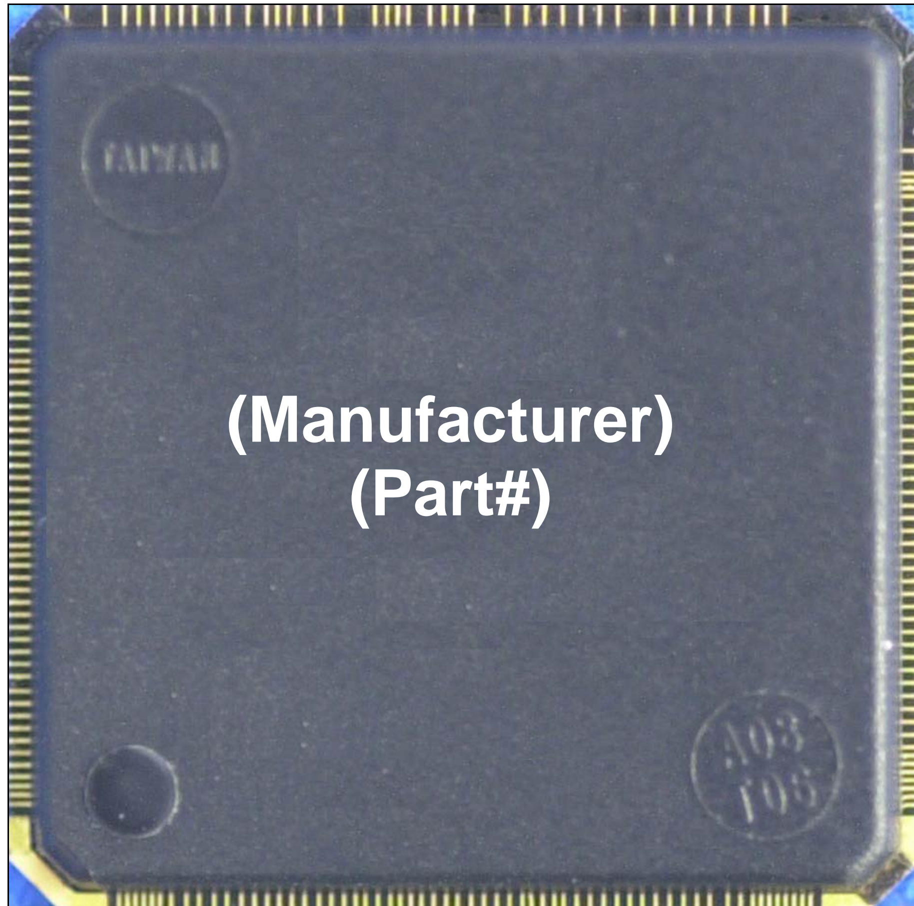
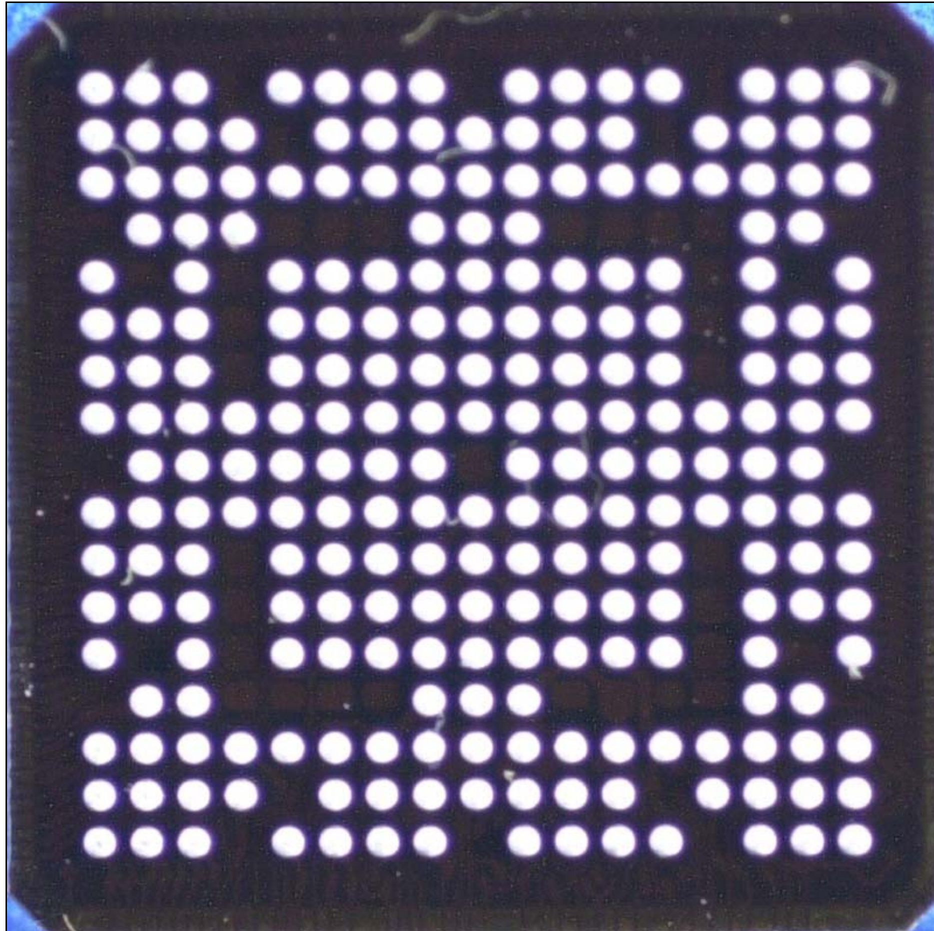
Device Summary Table

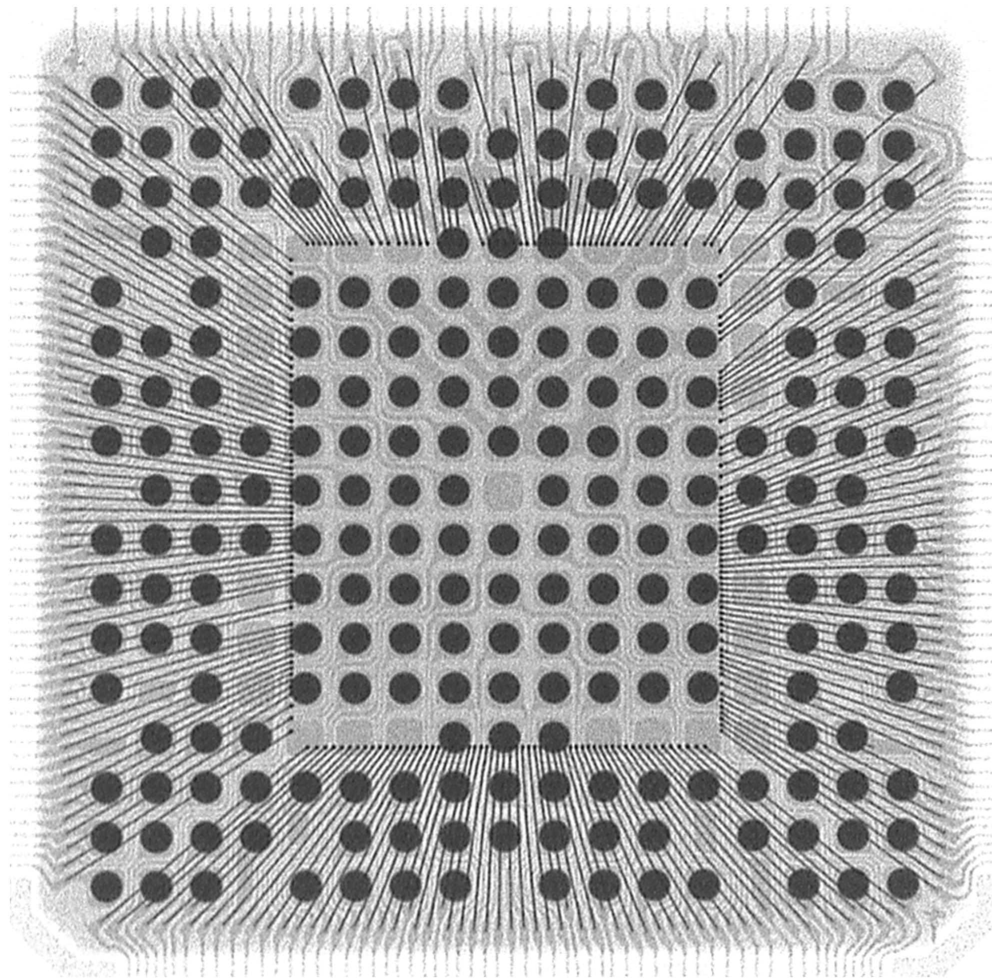
Manufacturer	(Company)
Part Number	Part#
Die Markings	Die Markings
Die Size	X.Xmm x X.Xmm = XX.XX mm^2
Number of Metal Levels	X
Number of Poly Levels	X
Interconnect Level Width / Pitch (µm)	
Metal Level - M1	X.XX / X.XX (Estimate)
Metal Level - M2	X.XX / X.XX (Estimate)
Metal Level - M3	X.XX / X.XX (Measured (X-Section))
Metal Level - M4	X.XX / X.XX (Measured (X-Section))
Metal Level - M5	X.XX / X.XX (Measured (X-Section))
Metal Level - M6	XX.XX / XX.XX (Measured (X-Section))
Poly Layer - P1	X.XX/ Not Specified (X-Section))
Process Type	CMOS (Copper)
Process Generation	X.XX µs
Transistor Gate Length	X.XX µs
Cell Size	X.XX μm^2



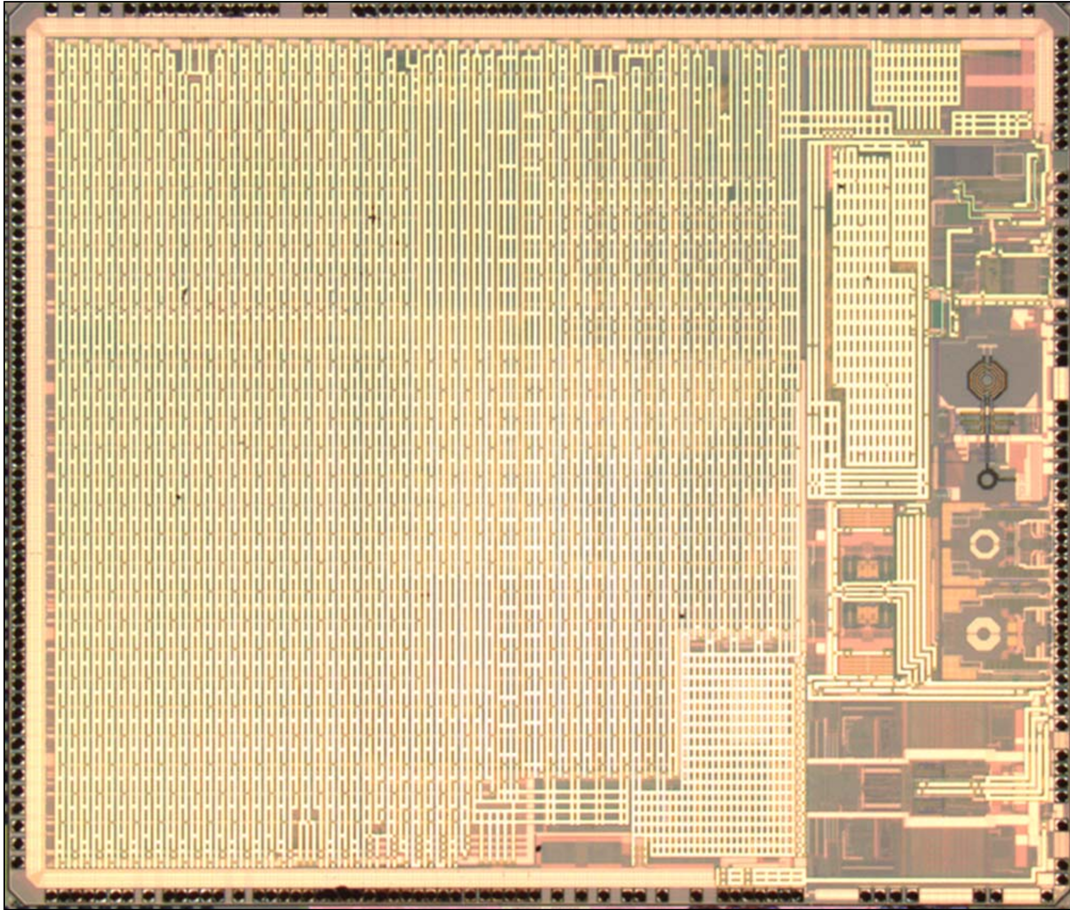
Package (top).



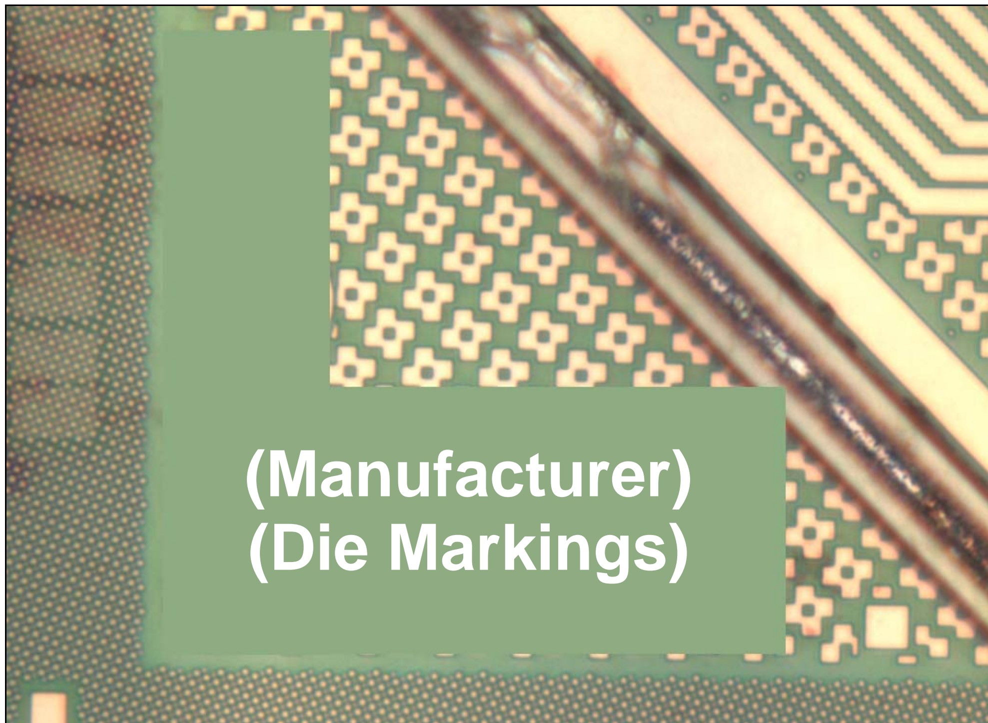
Package (bottom).



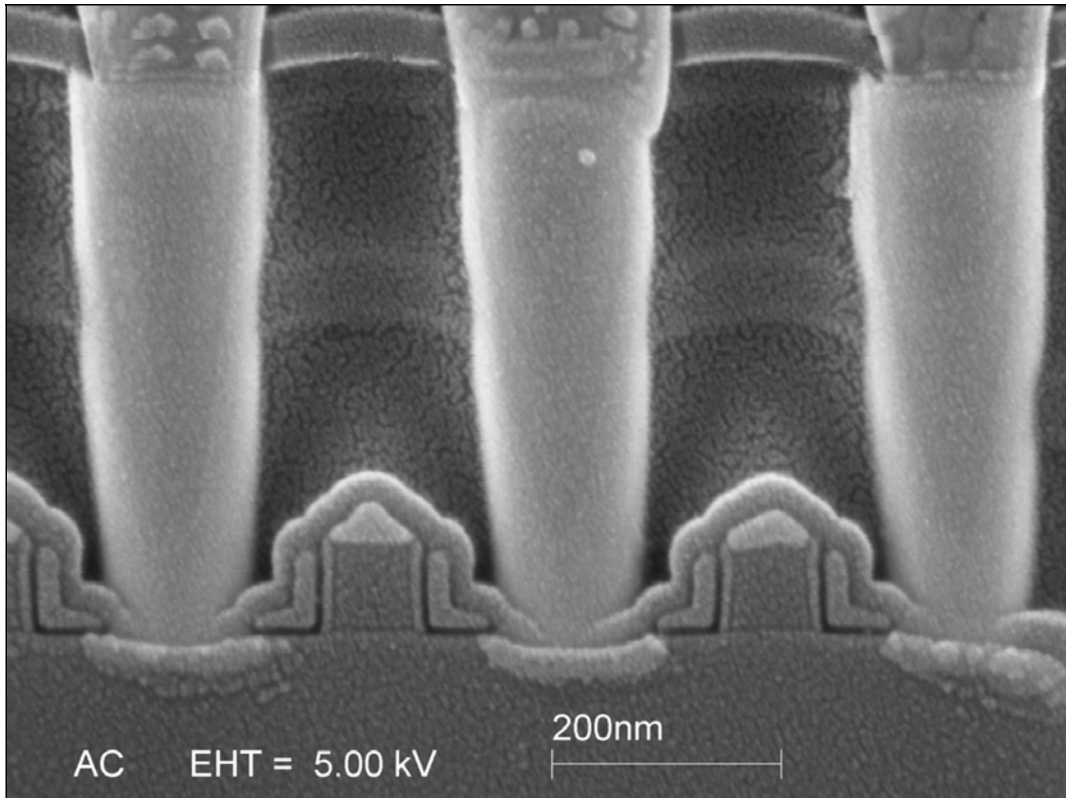
Package x-ray.



Die photograph.



Die markings.



SEM cross-section.